CAVU AEROSPACE UK

EDGE-64

PIC64-HPSC SPACEVPX SINGLE BOARD COMPUTER

HIGH-RELIABILITY EDGE COMPUTE FOR NEXT-GENERATION SPACECRAFT AUTONOMY

PIONEERING SPACECRAFT COMPUTING — BUILT ON NASA-HERITAGE HPSC

Edge-64 is a 3U SpaceVPX Onboard Computer built on Microchip's PIC64-HPSC architecture, delivering high-performance RISC-V vector compute with deterministic TSN Ethernet switching, PCIe Gen3/CXL-capable expansion, and SpaceWire connectivity for modern spacecraft avionics and payload processing.

✓ AUTONOMY-READY COMPUTE

8× RISC-V vector cores + integrated system controller for mixed-criticality architectures.

✓ DETERMINISTIC HIGH-SPEED NETWORKING

TSN Ethernet switching fabric plus low-latency data movement features for multi-SBC scaling.

MICROCHIP PIC64 HPSC

✓ PAYLOAD-GRADE I/O

PCIe Gen3 expansion, SpaceWire & storage options to match mission data profiles.

✓ RADIATION-TOLERANT ROADMAP

RT and RH device classes to align cost/assurance with mission needs.

KEY FEATURES

PROCESSOR: PIC64-HPSC1000 / PIC64-HPSC1100

8× RISC-V SiFive® X280 vector cores + S7 system controller

PERFORMANCE: ~26K DMIPS class; up to 2 TOPS (INT8) / 1 TFLOPS (bf16) (device-level headline)

MEMORY / STORAGE: DDR4 ECC; eMMC / NAND / NOR / QSPI; MRAM/FRAM options

HIGH-SPEED I/O: 10GbE/TSN, PCIe Gen3 ×8 (CXL-capable at silicon level)

SPACEWIRE: up to 7 ports (RMAP-compatible; 10–200 Mbps)

SOFTWARE: Linux®, RTEMS, Xen / partitioning support

SECURITY / PARTITIONING: hardware domain isolation (WorldGuard) for mixed-criticality workloads

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SPECIFICATIONS

PROCESSOR / COMPUTE

- PIC64-HPSC1000 / PIC64-HPSC1100 family (RISC-V vector compute)
- Mixed-criticality support via hardware partitioning (WorldGuard domains)
- Virtualization / safety architectures supported (project dependent)

MEMORY / STORAGE (CONFIGURABLE)

- DDR4 ECC memory, up to 16 GB
- Boot & mass-memory options: QSPI/NOR, NAND, MRAM/FRAM
- Optional "multiple image / boot region" architecture

HIGH-SPEED NETWORKING / FABRICS

- TSN Ethernet switch fabric (up to 240 Gbps aggregate switching capability)
- Low-latency multi-node scaling via RDMA over Converged Ethernet (RoCEv2) (where implemented)
- PCIe Gen3 expansion (x8 option); silicon supports CXL 2.0 capability

SPACECRAFT INTERFACES

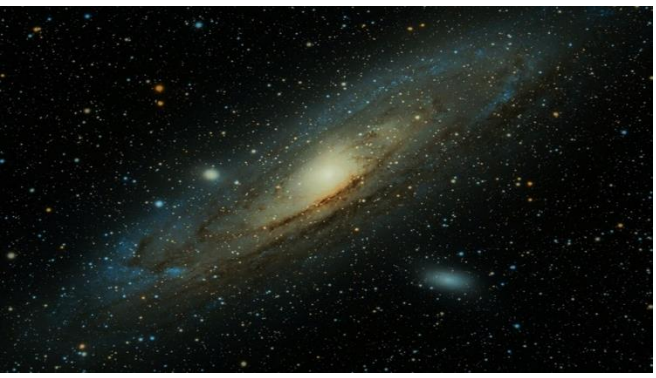
- SpaceWire ports (RMAP-compatible; internal routing at silicon level)
- Additional mission I/O via VPX backplane mapping and mezzanine/expansion options

RADIATION

- Radiation-Tolerant (RT): ~50 krad (Si) TID class
- Radiation-Hardened (RH): ~100 krad (Si) TID class

DELIVERABLES

- SBC + conduction plate / housing
- Software enablement package (BSP/boot chain per program scope)
- ICD / pin mapping + bring-up notes



BUDGET

- Form factor: 3U SpaceVPX
- Dimensions: ~100 × 160 × 25 mm
- Mass: ~650 g incl. conduction plate & housing
- Power: 8–15 W; up to 25 W peak

APPLICATIONS

- Deterministic Spacecraft Data Backbone Node
- Onboard Payload Processing and High-Rate Sensor Ingest
- Autonomous Surface Operations (Lunar/Mars Rovers, Landers, Habitats)
- Precision Landing, Terrain Relative Navigation, and Hazard Avoidance Compute
- Distributed / Clustered Avionics (Multi-SBC Scaling with RDMA/RoCEv2)
- High-Reliability Fault-Managed Platform Services (FDIR, Health Monitoring, Supervisory Control)

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