

OBC-PF-VPX

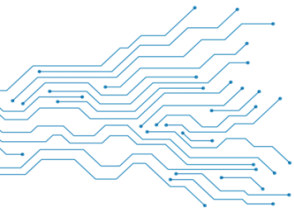
POLARFIRE SPACE VPX SINGLE BOARD COMPUTER

3U SpaceVPX System Controller

PolarFire® SoC

VITA 78

SOSA - Aligned



The OBC-PF- VPX is a 3U SpaceVPX (VITA 78) System Controller built on the Microchip PolarFire® SoC (MPFS460T / MPFS460TS). Its flash-based FPGA architecture provides ZeroFIT single-event upset immunity without the scrubbing or EDAC overhead inherent to SRAM-based devices. Twenty firmware-configurable SERDES lanes and 20 GB of ECC-protected memory support a single hardware baseline for Command and Data Handling, high-rate payload data recording, and protocol bridging — mission personality is selected through firmware with no hardware changes.

Device	Microchip MPFS460T-1FCG1152I / MPFS460TS-1FCG1152I (with security)
RISC-V Cores	Quad 64-bit U54 application cores + 1× E51 monitor core — >4,000 DMIPS total
FPGA Fabric	461k logic elements, 784 DSP blocks — flash-based, no SRAM bitstream
VectorBlox™	Up to 279 GOPs INT8 (V1000 config, no TMR) / 156 GOPs with synthesised TMR; scalable to >1 TOPS with multi-card deployment; 2–3× more power-efficient than competing FPGA inference engines; supports TensorFlow, ONNX
SERDES	20 lanes at up to 12.7 Gbps each — PCIe Gen2, 10G XFI, JESD204B, SATA III, Aurora — lane assignment firmware-selectable
PCIe	Gen2 ×4 hard block (expansion plane); PCIe switch payload card available for multi-slot fan-out
SEU / TID	ZeroFIT SEU-immune; >30 krad (Si) TID; latch-up immune; SECDED BRAM ECC
Operating temp.	–40°C to +85°C conduction-cooled (VITA 48.2)
FDIR	Hardware watchdog timer; dual-redundant on-card DC-DC regulators

PROCESSOR



KEY FEATURES

Flash-Based FPGA

ZeroFIT SEU-immune — no scrubbing or EDAC maintenance overhead

20 SERDES Lanes

PCIe Gen2, 10G XFI, JESD204B, SATA III — firmware-selectable per lane

20 GB Usable Memory

16 GB ECC DDR4 + 4 GB LPDDR4 — full SECDED protection on DDR4

>4,000 DMIPS

Quad 64-bit RISC-V application cores + 1 monitor core on PolarFire® SoC

>30 krad TID

ZeroFIT SEU-immune, latch-up immune, SECDED BRAM ECC

VectorBlox™ AI

On-fabric CNN: up to 279 GOPs INT8; scalable to >1 TOPS with multi-card deployment

SpaceVPX VITA 78

SLT3-CTL System Controller, SOSA Space Aligned

512 GB eMMC Storage

2× 256 GB — redundant non-volatile mass storage

Dual QSPI + MRAM

Triple-mode config store, zero-wear NV registers

Dual-String Ready

Active/standby fault-tolerance via SpaceUM-Polar

3–5 W Nominal

Conduction-cooled VITA 48.2 — 7 W peak

Firmware Personalities

OBC (CDH), recorder, or protocol bridge — single hardware baseline

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MEMORY & STORAGE

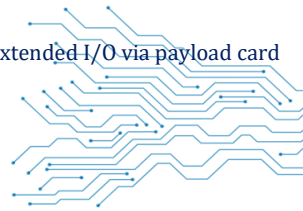


DDR4 — Fabric	16 GB ECC-protected (18 GB physical, ×72 SECDED ECC) at DDR4-1600 — 12.8 GB/s peak
LPDDR4	4 GB — 20 GB total usable memory (DDR4 + LPDDR4)
eMMC	512 GB (2× 256 GB) — redundant non-volatile mass storage
QSPI NOR Flash	2× 512 Mbit — primary and redundant boot / configuration store
MRAM (SPI)	4 Mbit — radiation-hard, zero-wear non-volatile register store

INTERFACES — Via VITA-46 MULTIGIG RT2 Backplane Connector

Three front-panel connectors: GigE (RJ45), SpaceWire (Micro-D 9), I/O / Debug (Micro-D 25 — UART, CAN, GPIO, JTAG, USB). Interfaces route via P0/J0, P1/J1, and P2/J2 backplane connector segments.

SERDES — Data Plane	≤10 lanes	Fat/Thin Pipe to payload slots; Aurora, 10GBASE-R XFI, or user-defined protocol
SERDES — PCIe	4 lanes	Gen2 ×4 hard block — expansion plane; switch payload card for multi-slot fan-out
SERDES — Spare	≥6 lanes	User-assignable: SATA III, JESD204B, 10GigE, inter-OBC sync
SpaceWire	4 ports (BP)	FPGA fabric LVDS; ECSS-E-ST-50-12C / RMAP control plane; additional ports via I/O payload card
GigE Ethernet	2 ports	Hard MAC SGMII; one port also accessible via front-panel RJ45 connector
CAN 2.0 B	2–4 ports	Hard CAN; primary ports exposed via front-panel Micro-D; extended capacity via I/O card
RS-422 / RS-485	2–8 ports	UART + line drivers; full / half-duplex; via front-panel Micro-D and / or I/O payload card
RS-232 / UART	2–4 ports	Hard UART
SPI / I2C	2–4 each	Masters: MRAM, QSPI, sensors, management bus; extended I/O via payload card
USB 2.0	1 port	Debug and firmware update; accessible via front-panel Micro-D
GPIO / ADC	20–60 / 8–16	Fabric GPIO (PWM-capable, discrete); 12/ 16-bit ADC housekeeping; extended I/O via payload card



BUDGET

Form factor	3U SpaceVPX (VITA 78)
Dimensions	100 × 160 mm (220 mm depth option)
SpaceVPX slot	SLT3-CTL — System Controller
Connector	VITA-46 MULTIGIG RT2
Front panel	GigE (RJ45), SpaceWire (Micro-D 9), I/O / Debug (Micro-D 25)
Cooling	Conduction-cooled, VITA 48.2
Power supply	5 V from backplane (P0/J0)
Power nominal	3–5 W Peak 7 W
Mass	~120 g (PCB); 500–650 g with enclosure & wedge-lock rails

SOFTWARE

OS support	Linux, FreeRTOS, RTEMS, INTEGRITY, FreeBSD, metal RISC-V HAL
Personalities	OBC (CDH), Recorder (SATA/NVMe via SERDES (protocol conversion))
AI inference	VectorBlox™ SDK — TensorFlow / ONNX; no FP design expertise required

COMPANION MODULES

PolarStore-2S	SATA Storage	2-drive SATA SSD payload module — 4 TB total; SERDES-driven from OBC backplane data plane
PolarStore-4S	SATA Storage	4-drive SATA SSD payload module — 8 TB total; high-capacity recorder configuration
PolarStore-2N	NVMe Storage	2-drive NVMe SSD payload module — up to 8 TB total; low-latency direct-attach
PolarStore-4N	NVMe Storage	4-drive NVMe SSD payload module — up to 16 TB total; maximum-capacity recording
SpaceUM-Polar	Utility	Dual-string power / clock / reset switching — LCL per slot, up to 5 modules
PSU-Polar-3U	Power	VITA 62-aligned 3U SpaceVPX power supply card
SpaceVPX-BP-SS	Backplane	Single-string 3U SpaceVPX backplane — 4 to 5 slots
SpaceVPX-BP-DS	Backplane	Dual-string 3U backplane — 8 slots; dual OBC + SpaceUM for full redundancy
SpaceVPX-CHX	Chassis	Conduction-cooled aluminium chassis — 4, 6, or 8-slot variants



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